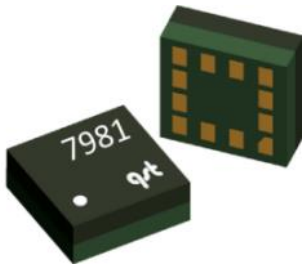
Abstract
Single-Chip 3-Axis Accelerometer QMA7981

Advanced Information



The QMA7981 is a single chip three-axis accelerometer. This surface-mount, small sized chip has integrated acceleration transducer with signal conditioning ASIC, sensing tilt, motion, shock and vibration, targeted for applications such as screen rotation, step counting, sleep quality, gaming and personal navigation in mobile and wearable smart devices.

The QMA7981 is based on our state-of-the-art, high resolution single crystal silicon MEMS technology. Along with custom-designed 14-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, and offset trimming. The I²C serial bus allows for easy interface.

The QMA7981 is in a 2x2x0.95mm3 surface mount 12-pin land grid array (LGA) package.

FEATURES

- 3-Axis Accelerometer in a 2x2x0.95 mm^3 Land Grid Array Package (LGA), guaranteed to operate over a temperature range of -40 °C to +85 °C.
- 14-Bit ADC with low noise accelerometer sensor
- I^2C Interface with Standard and Fast modes.
- Built-In Self-Test
- Wide range operation voltage (1.71V To 3.6V) and low power consumption (2-50μA low power conversion current)
- RoHS compliant , halogen-free
- Built–in motion algorithm

BENEFIT

- Small size for highly integrated products. Signals have been digitized and factory trimmed.
- High resolution allows for motion and tilt sensing
- High-Speed Interfaces for fast data communications.
- Enables low-cost functionality test after assembly in production
- Automatically maintains sensor's sensitivity under wide operation voltage range and compatible with battery powered applications
- Environmental protection and wide applications
- Low power and easy applications including step counting, sleep quality, gaming and personal navigation

CONTENTS

1 INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

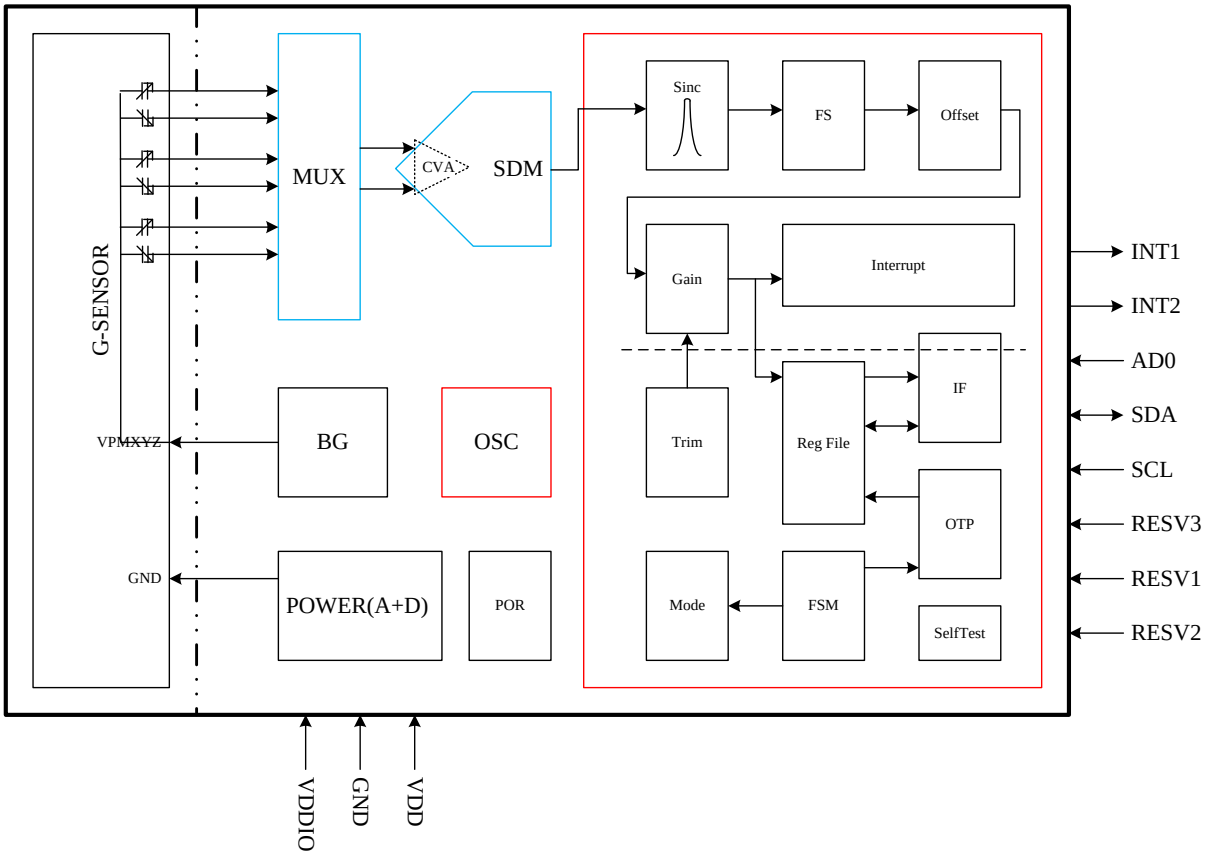


Figure 1. Block Diagram

Table 1. Block Function

Block	Function
Transducer	3-axis acceleration sensor
CVA	Charge-to-Voltage amplifier for sensor signals
Interrupt	Digital interrupt engine, to generate interrupt signal on data conversion, and motion function
FSM	Finite state machine, to control device in different mode
I^2C	Interface logic data I/O
OSC	Internal oscillator for internal operation
Power	Power block, including LDO

2 SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (* Tested and specified at 25°C and 3.0V VDD except stated otherwise.)

Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage VDD	VDD, for internal blocks	1.71	3.3	3.6	V
I/O voltage VDDIO	VDDIO, for IO only	1.71	3.3	VDD	V
Standby current	VDD and VDDIO on		1		μA
Low power current	ODR=268 Hz		50		μA
Low power current	ODR=134 Hz		25.3		μA
Low power current	ODR=67 Hz		12.9		μA
Low power current	ODR=33.6 Hz		6.7		μA
Low power current	ODR=13.4 Hz		2.9		μA
Low power current	ODR=6.7 Hz		1.7		μA
Low noise current	ODR=32.5 Hz		100		μA
Low noise current	ODR=21.6 Hz		83.3		μA
Low noise current	ODR=13 Hz		50		μA
Low noise current	ODR=6.5 Hz		25		μA
BW	Programmable bandwidth		0.16~336		Hz
Data output rate (ODR)	2*BW		0.32~672		Samples /sec
Startup time	From the time when VDD reaches to 90% of final value to the time when device is ready for conversion		2		ms
Wakeup time	From the time device enters into active mode to the time device is ready for conversion		1		ms
Operating temperature		-40		85	℃
Acceleration Full Range			±2/±4/±8/ ±16/±32		g
Sensitivity	FS=±2g		4096		LSB/g
Sensitivity	FS=±4g		2048		LSB/g
Sensitivity	FS=±8g		1024		LSB/g
Sensitivity	FS=±16g		512		LSB/g
Sensitivity	FS=±32g		256		LSB/g
Sensitivity Temperature Drift	FS=±2g, Normal VDD Supplies		±0.02		%/℃
Sensitivity tolerance	Gain accuracy		±4		%
Zero-g offset	FS=±2g, Normal VDD Supplies		±80		mg
Zero-g offset Temperature Drift	FS=±2g, Normal VDD Supplies		±2		mg/℃
Noise density	FS=±2g, run state		200		μg/sqrtHz
Nonlinearity	FS=±2g, Best fit straight line,		±0.5		%FS
Cross Axis Sensitivity			1		%

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (Tested at 25°C except stated otherwise.)

Parameters	Condition	Min	Max	Units
VDD		-0.3	5.4	V
VDDIO		-0.3	5.4	V
ESD	HBM		2	kV
Shock Immunity	Duration < 200μS		10000	g
Storage temperature		-50	150	℃

2.3 I/O Characteristics

Table 4. I/O Characteristics

Parameter	Symbol	Pin	Condition	Min.	TYP.	Max.	Unit
Voltage Input High Level 1	$V_{IH}1$	SDA, SCL		0.7*VDDIO		VDDIO+0.3	V
Voltage Input Low Level 1	$V_{IL}1$	SDA, SCL		-0.3		0.3*VDDIO	V
Voltage Output High Level	V_{OH}	INT1, INT2	Output Current ≥-100μA	0.8*VDDIO			V
Voltage Output Low Level	V_{OL}	INT1, INT2, SDA	Output Current ≤100μA(INT) Output Current ≤1mA (SDA)			0.2*VDDIO	V

3 PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of g field that generates a positive output reading in normal measurement configuration.

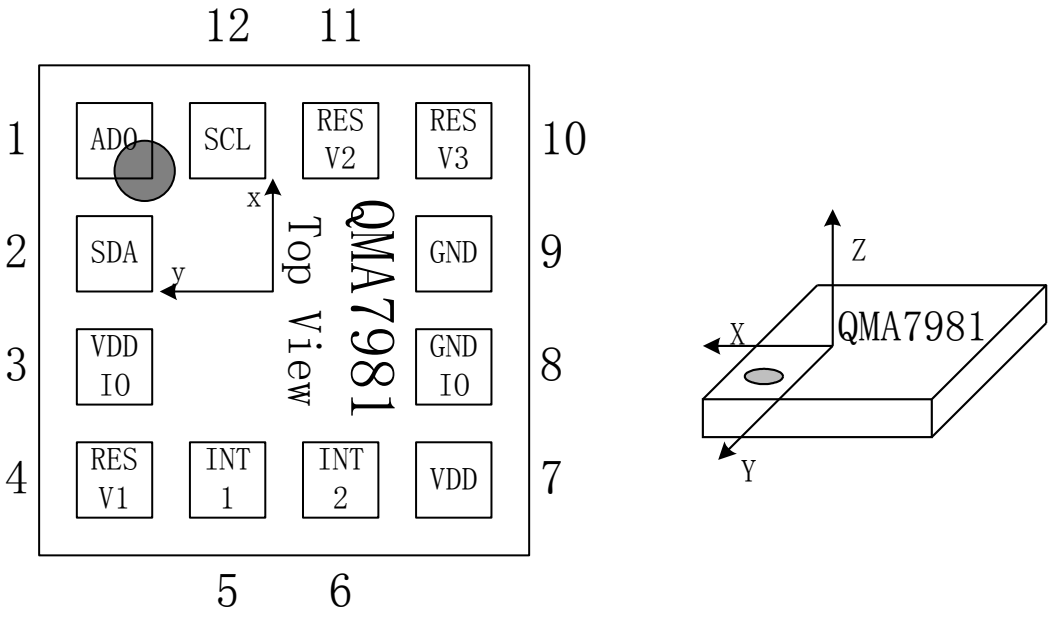


Figure 2. Package View

Table 5. Pin Configurations

PIN No.	PIN NAME	I/O	Power Supply	TYPE	Function
1	AD0	I	VDDIO	CMOS	LSB of I^2C address
2	SDA	IO	VDDIO	CMOS	Serial data for I^2C
3	VDDIO		VDDIO	Power	Power supply to digital interface
4	RESV1	I	VDDIO	CMOS	Reserved. Float or connect to GND
5	INT1	O	VDDIO	CMOS	Interrupt 1
6	INT2	O	VDDIO	CMOS	Interrupt 2
7	VDD		VDD	Power	Power supply to internal block
8	GNDIO		GND	Power	Ground to digital interface
9	GND		GND	Power	Ground to internal block
10	RESV3	IO	VDDIO	CMOS	Reserved
11	RESV2	IO	VDDIO	CMOS	Reserved
12	SCL	I	VDDIO	CMOS	Serial clock for I^2C

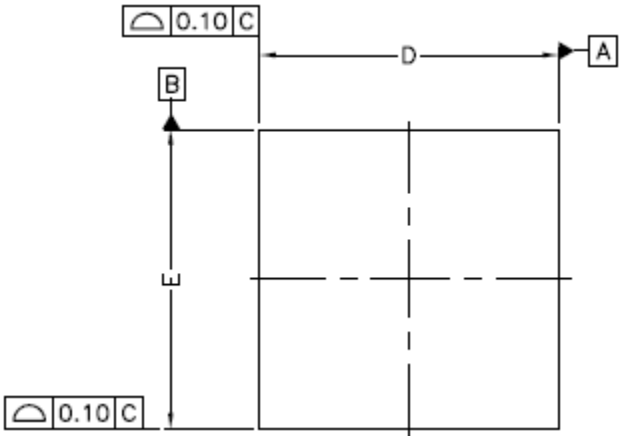
3.2 Package Outlines

3.2.1 Package Type

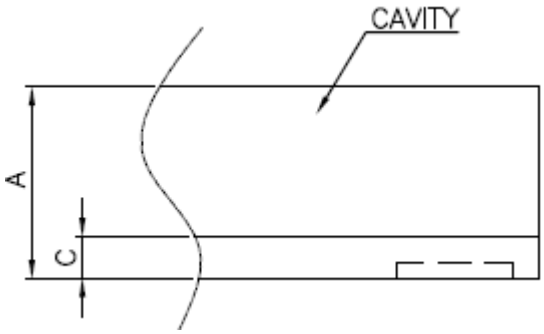
LGA (Land Grid Array)

3.2.2 Package Outline Drawing:

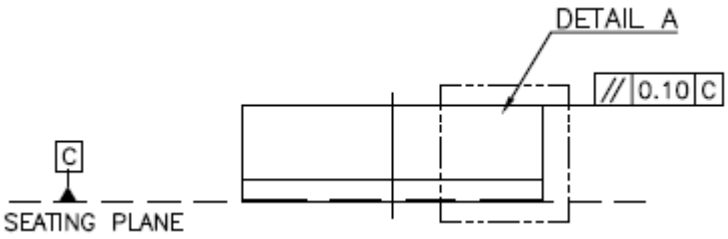
2.0mm (Length)*2.0mm (Width)*0.95mm (Height)



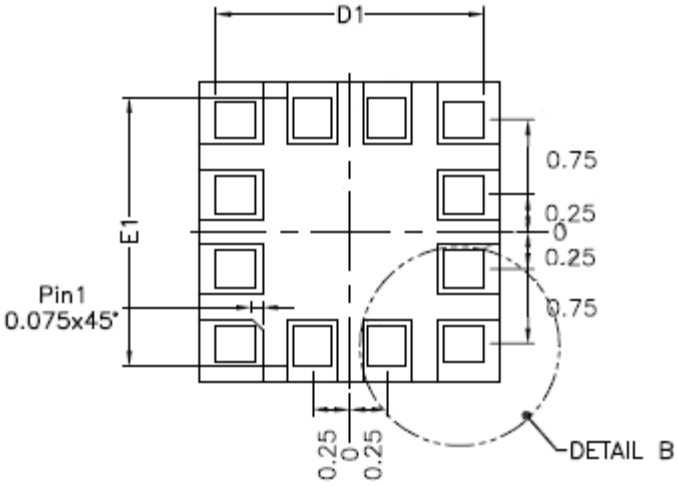
TOP VIEW



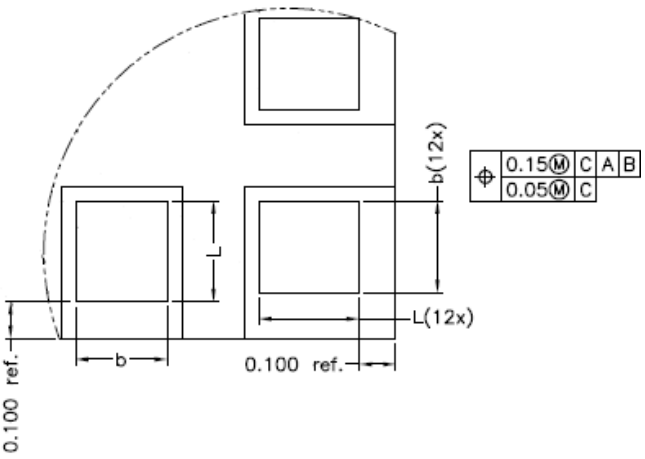
DETAIL A



SIDE VIEW



BOTTOM VIEW



DETAIL B

SYMBOL	DIMENSION (MM)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	0.95	1.00	0.035	0.037	0.039
C	0.16	0.20	0.24	0.006	0.008	0.009
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D1	1.80 BSC			0.071 BSC		
E	1.95	2.00	2.05	0.077	0.079	0.081
E1	1.80 BSC			0.071 BSC		
L	0.225	0.275	0.325	0.010	0.012	0.014

NOTE:
1. CONTROLLING DIMENSION: MILLIMETER.

Figure 3. Package Outline Drawing

3.2.3 Marking:

Figure 4. Marking Format

Marking Text	Description	Comments
Line 1	Product Name	“7981” stand for QMA7981
Line 2	Y: the last digital of year CCC: lot code	Lot code: 3 alphanumeric digits, variable to generate mass production trace-code
Line 3	P: Part number S: Sub-con ID	P: 1 alphanumeric digit, variable to identify part number S: 1 alphanumeric digit, variable identify sub-con
●	Pin 1 identifier	--

4 EXTERNAL CONNECTION

4.1 Dual Supply Connection

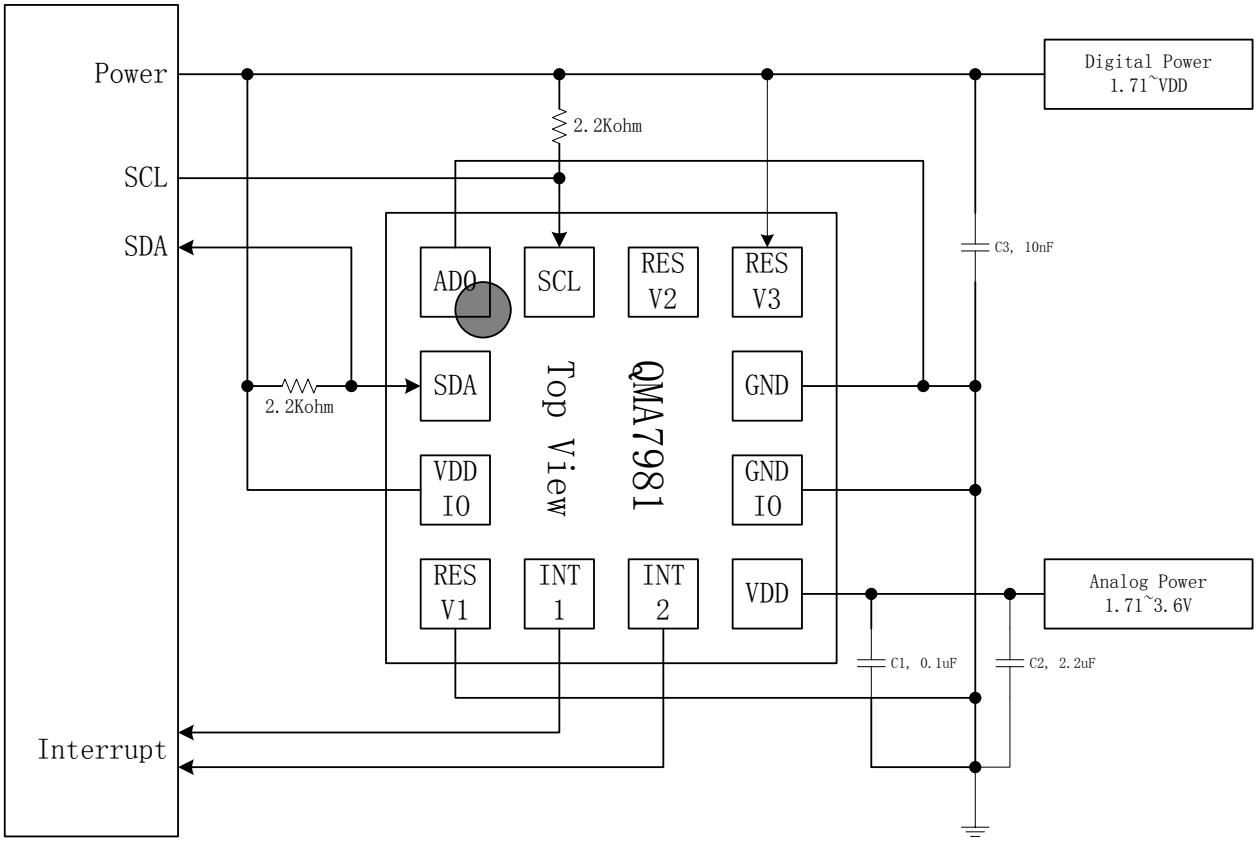


Figure 5. Dual Supply Connection

4.2 Single Supply connection

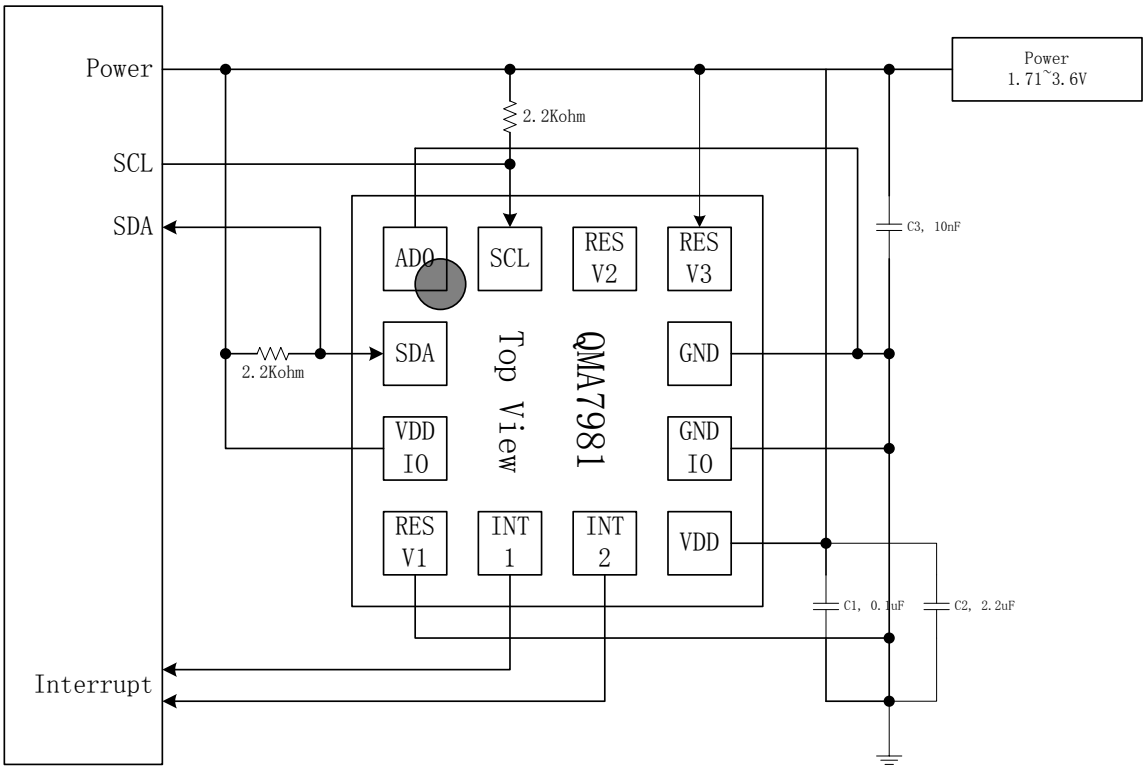


Figure 6. Single Supply Connection

5 BASIC DEVICE OPERATION

5.1 Acceleration Sensors

The QMA7981 acceleration sensor circuit consists of tri-axial sensors and application specific support circuits to measure the acceleration of device. When a DC power supply is applied to the sensor, the sensor converts any accelerating incident in the sensitive axis directions to charge output.

5.2 Power Management

Device has two power supply pins. VDD is the main power supply for all of the internal blocks, including analog and digital. VDDIO is a separate power supply, for digital interface only.

The device contains a power-on-reset generator. It generates reset pulse as power on, which can load the register's default value, for the device to function properly.
To make sure the POR block functions well, we should have such constrains on the timing of VDD and VDDIO.

The device should turn-on both power pins in order to operate properly. When the device is powered on, all registers are reset by POR, then the device transits to the standby mode and waits for further commends.

Table 6 provides references for four power states.

Table 6. Power States

Power State	VDD	VDDIO	Power State description
1	0V	0V	Device Off, No Power Consumption
2	0V	1.71v~3.6v	Not allowed. User need to make sure that VDDIO is less than VDD. Otherwise, there will be leakage from VDDIO to VDD through internal ESD devices
3	1.71v~3.6v	0	Device Off, Same Current as Standby Mode
4	1.71v~3.6v	1.71v~VDD	Device On, Normal Operation Mode, Enters Standby Mode after POR

5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), typically 50 milli-second. However it isn't controlled by the device. The Power–On–Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7

Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
POR Completion Time	PORT	Time Period After VDD and VDDIO at Operating Voltage to Ready for I^2C Commend and Analogy Measurement.			250	μs
Power off Voltage	SDV	Voltage that Device Considers to be Power Down.			0.2	V
Power on Interval	PINT	Time Period Required for Voltage Lower Than SDV to Enable Next POR	100			μs
Power on Time	PSUP	Time Period Required for Voltage from SDV to 90% of final value			50	ms

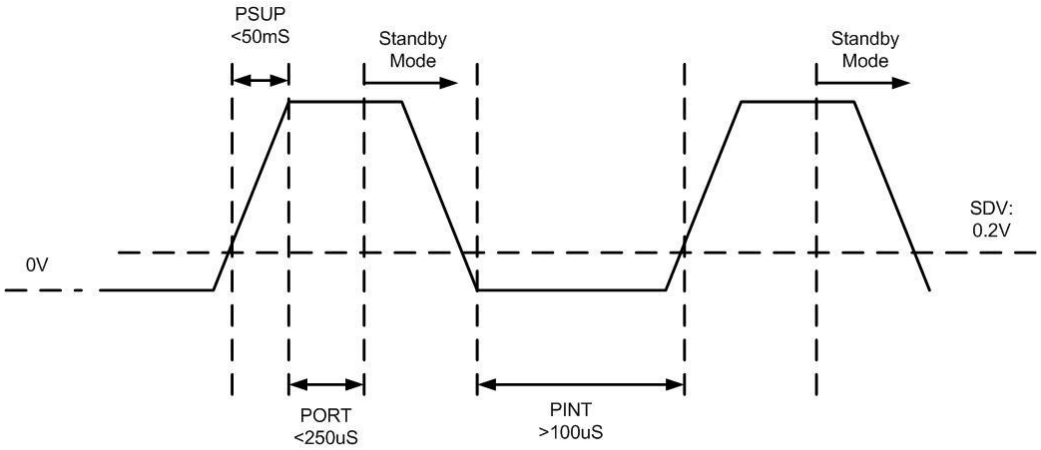


Figure 7. Power On/Off Timing

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C -Bus Specification, document number: 9398 393 40011. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100 kHz and 400 kHz, respectively. External pull-up resistors are required to support all these modes.

There are two I²C addresses selected by connecting pin 1 (AD0) to GND or VDDIO. The first six MSB are hardware configured to "001001" and the LSB can be configured by AD0.

Table 8. I²C Address Options

AD0 (pin 1)	I²C Slave Address(HEX)	I²C Slave Address(BIN)
Connect to GND	12	0010010
Connect to VDDIO	13	0010011

6 MODES OF OPERATION

6.1 Modes Transition

QMA7981 has two different operational modes, controlled by register (0x11), MODE_BIT. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I²C commands. The default mode after power-on is standby mode.

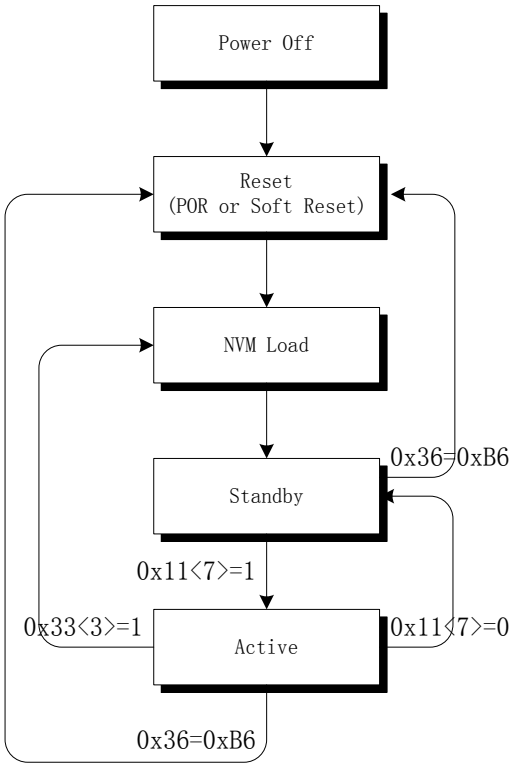


Figure 8. Basic operation flow after power-on

The default mode after power on is standby mode. Through I^2C instruction, device can switch between standby mode and active mode. With SOFTRESET by writing 0xB6 into register 0x36, all of the registers will get default values. SOFTRESET can be done both in active mode and in standby mode. Also, by writing 1 in NVM_LOAD (0x33<3>) when device is in active mode, the NVM related image registers will get default value from NVM, however, other registers will keep the values of their own.

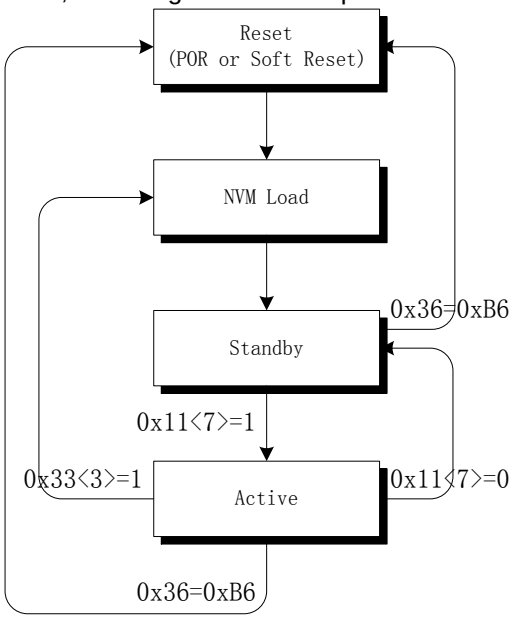


Figure 9. The work mode transferring

6.2 Description of Modes

6.2.1 Active Mode

In active mode, the ADC digitizes the charge signals from transducer, and digital signal processor conditions these signals in digital domain, processes the interrupts, and send data to Data registers (0x01~0x06).

6.2.2 Standby Mode

In standby mode, most of the blocks are off, while device is ready for access through I^2C. Standby mode is the default mode after power on or soft reset. Device can enter into this mode by set the soft reset register (0x36) to 0xB6 or set the MODE_BIT (0x11<7>) to logic 0.
Besides the above two modes, the device also contains NVM loading state. This state is used to reset the value of the NVM related image registers. There are two bits related to this state. When NVM_LOAD (0x33<3>) is set to 1, NVM loading starts. When the device is in NVM loading state, NVM_RDY (0x33<2>) is set to logic 0 by device. After NVM loading is finished, NVM_RDY (0x33<2>) is set back to logic 1 by device, and NVM_LOAD is reset to 0 by device automatically. NVM loading can only happen when NVM_LOAD is set to 1 in active mode. If the user sets this NVM_LOAD bit to 1 in standby mode, the device will not take the action until it enters into active state by setting MODE_BIT (0x11<7>) to logic 1.
After loading NVM, the device will enter into standby mode directly.
The loading time for NVM is about 100uS.

7 Functions and interrupts

ASIC support interrupts, such as STEP_INT, DRDY_INT

7.1 STEP_INT

The STEP/STEP_QUIT detect that the user is entering/exiting step mode. When the user enter into step mode, at least one axis sensor data will vary periodically, by numbering the variation periods the step counter can be calculated.

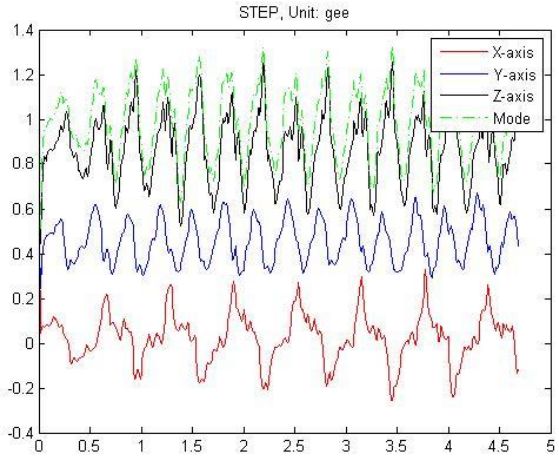


Figure 10. STEP/STEP_QUIT

Median data (max+min) /2 is called dynamic threshold, the max and min data can be updated by certainly samples, the sample number can be set by register STEP_SAMPLE_CNT (0x12<4:0>). When the sensor data decreasing (or increasing) through the dynamic threshold, a user run step is detected.
Register STEP_PRECISION (0x13<6:0>) is used as threshold when updating the new collected sensor data. Sensor data below the threshold will be discarded, this helps removing unstable variations causing failed detection.

The run step event happened at certain interval timing. All of the events outside the timing window will not be regarded as a run step and the step counter will not counted. The timing window can be set by register STEP_TIME_UP(0x15) and STEP_TIME_LOW(0x14), the conversion ODR numbers ranged from STEP_TIME_LOW *ODR to 8* STEP_TIME_UP*ODR . Also if no new run step event detected until the up limited timing threshold, STEP_QUIT INT will generation.
To remove unstable variation which will cause false STEP event detection, the step counter considers steps as valid step events only after 4 continuous steps detected. Also, the step counter register STEP_CNT_ / STEP_CNT_MSB (0x07,0x08) will be updated immediately by value 4, and interrupt STEP is also generated.

The related interrupt status bit is STEP_INT (0x0A<3>) and STEP_QUIT_INT (0x0A<2>). When the interrupt is generated, the value of STEP_INT/ STEP_QUIT_INT will be set to logic 1, which will be cleared after the interrupt status register is read by user. STEP_EN/STEP_QUIT_EN (0x16<3>/0x16<2>) is the enable bit for the STEP_INT/STEP_QUIT_INT. Also, to get this interrupt on PIN_INT1 and/or PIN_INT2, we need to set INT1_STEP (0x19<3>)/INT1_STEP_QUIT (0x19<2>) or INT2_STEP (0x1B<3>) /INT2_STEP_QUIT (0x1B<2>) to logic 1, to map the internal interrupt to the interrupt PINs.

7.2 DRDY_INT

The width of the acceleration data is 14 bits, in two's complement representation. The data of each axis is split into 2 parts, the MSB part (one byte contains bit 13 to bit 6) and the LSB part (one byte contains bit 5 to bit 0). Reading data should start with LSB part. When user is reading the LSB byte of data, to ensure the integrity of the acceleration data, the content of MSB can be locked, by setting SHADOW_DIS (0x21<6>) to logic 0. This lock function can be disabled by setting SHADOW_DIS to logic 1. Without lock, the MSB and LSB content will be updated by new value immediately. The bit NEW_DATA in the LSB byte is the flag of the new data. If new data is updated, this NEW_DATA flag will be 1, and will be cleared when corresponding MSB or LSB is read by user. Also, the user should note that even with SHADOW_DIS=0, the data of 3 axes are not guaranteed from the same time point.

The device supports four different acceleration measurement ranges. The range is setting through RANGE (0x0F<3:0>), and the details as following:

RANGE	Acceleration range	Resolution
0001	2g	244ug/LSB
0010	4g	488ug/LSB
0100	8g	977ug/LSB
1000	16g	1.95mg/LSB
1111	32g	3.91mg/LSB
Others	2g	244ug/LSB

The interrupt for the new data serves for the synchronous data reading for the host. It is generated after storing a new value of z-axis acceleration data into data register. This interrupt will be cleared automatically when the next data conversion cycle starts, and the interrupt will be effective about 64*MCLK, and automatically cleared.
The interrupt mode for the new data is fixed to be non-latched.

7.3 Interrupt configuration

The device has the above 3 interrupt engines. Each of the interrupts can be enabled and configured independently. If the trigger condition of the enabled interrupt fulfilled, the corresponding interrupt status bit will be set to logic 1, and the mapped interrupt pin will be activated. The device has two interrupt PINs, INT1 and INT2. Each of the interrupts can be mapped to either PIN or both PINs.

The interrupt status registers update when a new data word is written into the data registers. If an interrupt is disabled, the related active interrupt status bit is disabled immediately.

Device supports 2 interrupt modes, non-latched, and latched mode. The interrupt modes are set through LATCH_INT (0x21<0>).
In non-latched mode, the interrupt status bit and the mapped interrupt pin are cleared as soon as the associated conditions are no more valid, or read operation to the INT_STAT (0x09~0x0d). Exceptions to this are the new data, orientation, and flat interrupts, which are automatically reset after a fixed time.
In latched mode, the clearings of the interrupt status and selected pin are determined by INT_RD_CLR (0x21<7>). If INT_RD_CLR=0, read operation to the INT_STAT will clear the interrupt and the selected pin. If INT_RD_CLR=1, any read operation to the device will clear the interrupt and the selected pin.
If the condition for trigging the interrupt still holds, the interrupt status will be set again with the next change of the data registers.

Mapping the interrupt pins can be set by INT_MAP (0x19~0x1B).
The electrical interrupt pins can be set in INT_PIN_CONF (0x20<3:0>). The active logic level can be set to 1 or 0, and the interrupt pin can be set to open-drain or push-pull.

If the interrupt mode is configured as latched mode, the interrupt can also be cleared by I^2C reading any of the interrupt status register (0x09 ~ 0x0d).

8 I²C COMMUNICATION PROTOCOL

8.1 I²C Timings

Table 9 and Figure 11 describe the I²C communication protocol times

Table 9. I²C Timings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL Clock	f_{scl}		0		400	kHz
SCL Low Period	t_{low}		1			μs
SCL High Period	t_{high}		1			μs
SDA Setup Time	t_{sudat}		0.1			μs
SDA Hold Time	t_{hddat}		0		0.9	μs
Start Hold Time	t_{hdsta}		0.6			μs
Start Setup Time	t_{susta}		0.6			μs
Stop Setup Time	t_{susto}		0.6			μs
New Transmission Time	t_{buf}		1.3			μs
Rise Time	t_r					μs
Fall Time	t_f					μs

Figure 11. I²C Timing Diagram

8.2 I²C R/W Operation

8.2.1 Abbreviation

Table 10. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I²C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.
ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver mush then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.

NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.2.3 I²C Write

I²C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 11. I²C Write

START	Slave Address							R W	SACK	Register Address (0x11)								SACK	Data (0x80)								SACK	STOP
	0	0	1	0	0	1	0	0		0	0	0	1	0	0	0	1		1	0	0	0	0	0	0	0		

8.2.4 I²C Read

I²C write sequence consists of a one-byte I²C write phase followed by the I²C read phase. A start condition must be generated between two phase. The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.
The register address is automatically incremented and more than one byte can be sequentially read out. Once a new data read transmission starts, the start address will be set to the register address specified in the current I²C write command.

Table 12. I²C Read

START	Slave Address							R W	SACK	Register Address (0x00)								SACK										
	0	0	1	0	0	1	0	0		0	0	0	0	0	0	0	0											
START	Slave Address							R W	SACK	Data (0x00)								MACK	Data (0x01)									
	0	0	1	0	0	1	0	1		0	0	0	0	0	0	1	0		0	0	0	0	0	0	0	0		
MACK	Data (0x02)								MACK	…….								MACK	Data (0x07)								NACK	STOP
	0	0	0	0	0	0	1	0		…….									0	0	0	0	0	0	0	0		

9 REGISTERS

9.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses

Table 13. Register Map

Add.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W	DEF
0x3F										R	00
0x3E										RW	00
0x3D		GAIN_Z<7:0>								RW	NVM
0x3C		GAIN_Y<7:0>								RW	NVM
0x3B		GAIN_X<7:0>								RW	NVM
0x3A		OFFSET_Z<7:0>								RW	NVM
0x39		OFFSET_Y<7:0>								RW	NVM
0x38		OFFSET_X<7:0>								RW	NVM
0x37	IMAGE	OFFSET_X<10:8>			GAIN_Z<9:8>		OFFSET_Y<10:8>			RW	NVM
0x36	S_RESET	SOFTRESET: 0xB6 / NVM_UNLOCK: 0xB3								RW	00
0x35										R	FF
0x34										R	FF
0x33	NVM_CFG					NVM_LOAD	NVM_RDY	NVM_PROG	NVM_LOAD_DONE	RW	05
0x32	ST	SELFTEST_BIT					SELFTEST_SIGN			RW	00
0x31										RW	00
0x30										RW	3F
0x2F										RW	00
0x2E										RW	00
0x2D										RW	00
0x2C										RW	00
0x2B										RW	0A
0x2A										RW	04
0x29		OS_CUST_Z<7:0>								RW	00
0x28		OS_CUST_Y<7:0>								RW	00
0x27	OS_CUST	OS_CUST_X<7:0>								RW	00
0x26										RW	C0
0x25										RW	0F
0x24										RW	81
0x23										RW	30
0x22										RW	09
0x21	INT_CONF	INT_RD_CLR	SHADOW_DIS						LATCH_INT	RW	00
0x20	INT_PIN_CONF					INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	05
0x1F		STEP_START_CNT			STEP_COUNT_FILT<2:0>			STEP_AMP_SEL<1:0>		RW	00
0x1E										R	FF
0x1D	STEP_CONF	STEP_INTERVAL<7:0>								RW	00
0x1C					INT2_DATA					RW	00
0x1B			INT2_SIG_STEP			INT2_STEP				RW	00
0x1A					INT1_DATA					RW	00
0x19	INT_MAP		INT1_SIG_STEP			INT1_STEP				RW	00
0x18										RW	00
0x17					INT_DATA_EN					RW	00
0x16	INT_EN		SIG_STEP_EN			STEP_EN				RW	00
0x15		STEP_TIME_UP<7:0>								RW	00
0x14		STEP_TIME_LOW<7:0>								RW	00
0x13		STEP_CLR	STEP_PRECISION<6:0>							RW	00
0x12	STEP_CONF	STEP_START			STEP_SAMPLE_CNT<4:0>					RW	0C
0x11	PM	MODE_BIT		T_RSTB_SINC_SEL<1:0>		MCLK_SEL<3:0>				RW	00
0x10	BW				BW<4:0>					RW	00
0x0F	FSR					RANGE<3:0>				RW	00
0x0E										R	00
0x0D		STEP_CNT_OVFL								R	00
0x0C										R	00
0x0B					DATA_INT					R	00
0x0A			SIG_STEP			STEP_INT				R	00
0x09	INT_ST									R	00
0x08		STEP_CNT<15:8>								R	00
0x07	STEPCNT	STEP_CNT<7:0>								R	00
0x06		ACC_Z<13:6>								R	00
0x05		ACC_Z<5:0>							NEWDATA_Z	R	00
0x04		ACC_Y<13:6>								R	00
0x03		ACC_Y<5:0>							NEWDATA_Y	R	00
0x02		ACC_X<13:6>								R	00
0x01	DATA	ACC_X<5:0>							NEWDATA_X	R	00
0x00	CHIP_ID	CHIP ID to indicate the product version								R	ANA

9.2 Register Definition

Register 0x00 (CHIP ID)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
Device ID								RW	0xBX

This register is used to identify the device

Register 0x01 ~ 0x02 (DXL, DXM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DX<5:0>							NEWDATA_X	R	0x00
DX<13:6>								R	0x00

DX: 14bits acceleration data of x-channel. This data is in two's complement.
NEWDATA_X: 1, acceleration data of x-channel has been updated since last reading

0, acceleration data of x-channel has not been updated since last reading

Register 0x03 ~ 0x04 (DYL, DYM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DY<5:0>							NEWDATA_Y	R	0x00
DY<13:6>								R	0x00

DY: 14bits acceleration data of y-channel. This data is in two's complement.
NEWDATA_Y: 1, acceleration data of y-channel has been updated since last reading
0, acceleration data of y-channel has not been updated since last reading

Register 0x05 ~ 0x06 (DZL, DZM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DZ<5:0>							NEWDATA_Z	R	0x00
DZ<13:6>								R	0x00

DZ: 14bits acceleration data of z-channel. This data is in two's complement.
NEWDATA_Z: 1, acceleration data of z-channel has been updated since last reading
0, acceleration data of z-channel has not been updated since last reading

Register 0x07 ~ 0x08 (ID)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT<7:0>								R	0x00
STEP_CNT<15:8>								R	0x00

STEP_CNT<15:0> 16 bits of step counter

Register 0x0a (INT_STAT0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	SIG_STEP			STEP_INT				R	0x00

SIG_STEP: 1, significant step is active
0, significant step is inactive
STEP_INT: 1, step valid interrupt is active
0, step quit interrupt is inactive

Register 0x0b (INT_STAT1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			DATA_INT T					R	0x00

This register indicates interrupt status related to data ready.

DATA_INT: 1, data ready interrupt active
0, data ready interrupt inactive

Register 0x0d (INT_STAT4)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT_OVFL								R	0x00

STEP_CNT_OVFL: 1, step counter is over-flowed
0, step counter is not over-flowed

Register 0x0f (RANGE)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				RANGE<3:0>				RW	0x00

RANGE<3:0>: set the full scale of the accelerometer. Setting as following

RANGE<3:0>	Acceleration range	Resolution
0001	2g	244ug/LSB
0010	4g	488g/LSB
0100	8g	977ug/LSB
1000	16g	1.95mg/LSB
1111	32g	3.91mg/LSB
Others	2g	244ug/LSB

Register 0x10 (BW)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			BW<4:0>					RW	0x00

BW<4:0>: bandwidth setting, as following

BW<4:0>	DSR	ODR
xx000		
xx001		
xx010		
xx011		
xx100		
xx101	1024	MCLK/15378
xx110	256	MCLK/3858
xx111	128	MCLK/1938

Register 0x11 (PM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
MODE_BIT		T_RSTB_SINC_SEL<1:0>		MCLK_SEL<3:0>				RW	0x00

MODE_BIT: 1, set device into active mode
0, set device into standby mode

T_RSTB_SINC_SEL<1:0>: Reset clock setting. The preset time is reserved for CIC filter in digital
11, T_RSTB_SINC=8*MCLK
10, T_RSTB_SINC=6*MCLK
01, T_RSTB_SINC=4*MCLK
00, T_RSTB_SINC=3*MCLK

MCLK_SEL<3:0>: set the master clock to digital

MCLK_SEL<3:0>	Freq of MCLK
0000	500KHz
0001	333KHz
0010	200KHz
0011	100KHz
0100	50KHz
0101	25KHz
0110	12.5KHz
0111	5KHz
1xxx	Reserved

Register 0x12 (STEP_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_START			STEP_SAMPLE_COUNT<4:0>					RW	0x0C

STEP_START: start step counter, this bit should be set when using step counter
STEP_SAMPLE_COUNT<4:0>:
sample count setting for dynamic threshold calculation. The actual value is STEP_SAMPLE_COUNT<4:0>*4, default is 0xC, 48 sample count

Register 0x13 (STEP_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CLR	STEP_PRECISION<6:0>							RW	0x00

STEP_CLR: clear step count in register 0x7 and 0x8
STEP_PRECISION<6:0>:
threshold for acceleration change of two successive sample which is used to update sample_new register in step counter, the actual g value is TEP_PRECISION<6:0>*3.9mg

Register 0x14 (STEP_CONF2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME_LOW<7:0>								RW	0x00

STEP_TIME_LOW<7:0>: the short time window for a valid step, the actual time is STEP_TIME_LOW<7:0>*(1/ODR)

Register 0x15 (STEP_CONF3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME_UP<7:0>								RW	0x00

STEP_TIME_UP<7:0>: time window for quitting step counter, the actual time is STEP_TIME_UP<7:0>*8*(1/ODR)

Register 0x16 (INT_EN0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	SIG_STEP_EN			STEP_EN				RW	0x00

SIG_STEP_EN: 1, enable significant step interrupt
0, disable significant step interrupt
STEP_EN: 1, enable step valid interrupt
0, disable step valid interrupt

Register 0x17 (INT_EN1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			DATA_EN					RW	0x00

DATA_EN: 1, enable data ready interrupt
0, disable data ready interrupt

Register 0x19 (INT_MAP0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT1_SIG_STEP			INT1_STEP				RW	0x00

INT1_SIG_STEP: 1, map significant step interrupt to INT1 pin
0, not map significant step interrupt to INT1 pin
0, not map double tap interrupt to INT1 pin
INT1_STEP: 1, map step valid interrupt to INT1 pin
0, not map step valid interrupt to INT1 pin

Register 0x1a (INT_MAP1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			INT1_DATA					RW	0x00

INT1_DATA: 1, map data ready interrupt to INT1 pin
0, not map data ready interrupt to INT1 pin

Register 0x1b (INT_MAP2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT2_SIG_STEP			INT2_STEP			INT2_SIG_MOT	RW	0x00

INT2_SIG_STEP: 1, map significant step interrupt to INT2 pin
0, not map significant step interrupt to INT2 pin
INT2_STEP: 1, map step valid interrupt to INT2 pin
0, not map step valid interrupt to INT2 pin
INT2_SIG_MOT: 1, map significant interrupt to INT2 pin
0, not map significant interrupt to INT2 pin

Register 0x1c (INT_MAP3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
			INT2_DATA					RW	0x00

INT2_DATA: 1, map data ready interrupt to INT2 pin
0, not map data ready interrupt to INT2 pin

Register 0x1d (SIG_STEP_TH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_INTERVAL<7:0>								RW	0x00

STEP_INTERVAL <7:0>: threshold of significant step. When MOD(STEP_CNT, STEP_INTERVAL)=0, SIG_STEP_INT will be generated.

Register 0x1f (STEP)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_START_CNT			STEP_COUNT_FILT<2:0>			STEP_AMP_SEL<1:0>		RW	0x00

STEP_START_CNT: 1, start the step count when step pattern >=4

0, start the step count when step pattern >=8

STEP_COUNT_FILT<2:0>: not open to customer. Used for step count debug. Similar function as time-low. STEP_COUNT_FILT<2:0>*ODR < 100mS

STEP_AMP_SEL<1:0>: 11,not trigger the step count when peak-to-peak value <30*(16*LSB)
10,not trigger the step count when peak-to-peak value <150*(16*LSB)
01,not trigger the step count when peak-to-peak value <100*(16*LSB)
00,not trigger the step count when peak-to-peak value <50*(16*LSB)

Register 0x20 (INTPIN_CONF)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	0x05

INT2_OD: 1, open-drain for INT2 pin
0, push-pull for INT2 pin

INT2_LVL: 1, logic high as active level for INT2 pin
0, logic low as active level for INT2 pin

INT1_OD: 1, open-drain for INT1 pin
0, push-pull for INT1 pin

INT1_LVL: 1, logic high as active level for INT1 pin
0, logic low as active level for INT1 pin

Register 0x21 (INT_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT_RD_CLR	SHADOW_DIS						LATCH_INT	RW	0x00

INT_RD_CLR: 1, clear all the interrupts in latched-mode, when any read operation to this device
0, clear all the interrupts, only when read the register INT_STAT (0x0A~0x0B), no matter the interrupts in latched-mode, or in non-latched-mode

SHADOW_DIS: 1, disable the shadowing function for the acceleration data
0, enable the shadowing function for the acceleration data. When shadowing is enabled, the MSB of the acceleration data is locked, when corresponding LSB of the data is reading. This can ensure the integrity of the acceleration data during the reading. The MSB will be unlocked when the MSB is read.

LATCH_INT: 1, interrupt is in latch mode
0, interrupt is in non-latch mode

Register 0x27 (OS_CUST_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_X<7:0>								RW	0x00

OS_CUST_X<7:0>: offset calibration of X axis for user, the LSB depends on full-scale of the device which is 3.91mg in 2g range, 7.81mg in 4g range, 15.6mg in 8g range, 31.25mg in 16g range, 62.5mg in 32g range

Register 0x28 (OS_CUST_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Y<7:0>								RW	0x00

OS_CUST_Y<7:0>: offset calibration of Y axis for user, the LSB depends on full-scale of the device which is 3.91mg in 2g range, 7.81mg in 4g range, 15.6g in 8g range, 31.25mg in 16g range, 62.5mg in 32g range

Register 0x29 (OS_CUST_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Z<7:0>								RW	0x00

OS_CUST_Z<7:0>: offset calibration of Z axis for user, the LSB depends on full-scale of the device which is 3.91mg in 2g range, 7.81mg in 4g range, 15.6g in 8g range, 31.25mg in 16g range, 62.5mg in 32g range

Register 0x32 (ST)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
SELFTEST_BIT					SELFTEST_SIGN			RW	0x00

SELFTEST_BIT: 1, self-test enabled. When self-test enabled, a delay of 3ms is necessary for the value settling.
0, normal

SELFTEST_SIGN: 1, set self-test excitation positive
0, set self-test excitation negative

Register 0x33 (NVM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
				NVM_LOAD	NVM_RDY	NVM_PROG	NVM_LOAD_DONE	RW	0x05

NVM_LOAD: 1, trigger loading register from NVM
0, not trigger loading register form NVM
This bit is cleared when NVM loading is done

NVM_RDY: 1, NVM is ready, loading or programing NVM is done
0, NVM is not ready, loading or programming NVM is in progress.
NVM_RDY is read-only to customer.

NVM_PROG: 1, trigger programing NVM
0, not trigger programming NVM
This bit is cleared when NVM programming is done

NVM_LOAD_DONE: 1, NVM loading is done
0, NVM loading is not done

Register 0x37 (OFFSET_XY)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_X<10:8>			GAIN_Z<9:8>		OFFSET_Y<10:8>			RW	0x00

OFFSET_X<10:8>: offset value of x-channel. This data is the trimming data for x channel in FT phase, together with OFFSET_X<7:0> in 0x38.
GAIN_Z<9:8>: sensitivity trimming bits for z channel, together with GAIN_Z<7:0> in 0x3D (total 10 bits).
OFFSET_Y<10:8>: offset value of y-channel. This data is the trimming data for y channel in FT phase, together with OFFSET_Y<7:0> in 0x39.

Register 0x38 (OFFSET_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_X<7:0>								RW	0x00

OFFSET_X<7:0>: offset value of x-channel. This data is the trimming data for x channel in FT phase,
together with OFFSET_X<10:8> in 0x37<7:5>.
The trimming LSB is 3.91mg, the full trimming range in digital domain is +/-4g
User can perform read-modify-write access, to change the register value. However,
when device is re-power-on, or soft-reset, this value will be updated to default again.

Register 0x39(OFFSET_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_Y<7:0>								RW	0x00

OFFSET_Y<7:0>: offset value of y-channel. This data is the trimming data for y channel in FT phase, together with OFFSET_Y<10:8> in 0x37<2:0>.
The trimming LSB is 3.91mg, the full trimming range in digital domain is +/-4g
User can perform read-modify-write access, to change the register value. However, when device is re-power-on,
Or soft-reset, this value will be updated to default again.

Register 0x3a (OFFSET_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OFFSET_Z<7:0>								RW	0x00

OFFSET_Z<7:0>: offset value of z-channel. This data is the trimming data for z channel in FT phase, together with OFFSET_Z<11:8> in 0x45<3:0>.
The trimming LSB is 3.91mg, the full trimming range in digital domain is +/-8g
User can perform read-modify-write access, to change the register value. However, when device is re-power-on,
or soft-reset, this value will be updated to default again.

Register 0x3b (GAIN_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
GAIN_X<7:0>								RW	0x00

GAIN_X<7:0>: sensitivity trimming bits for x channel (total 8 bits).

Register 0x3c (GAIN_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
GAIN_Y<7:0>								RW	0x00

GAIN_Y<7:0>: sensitivity trimming bits for y channel (total 8 bits).

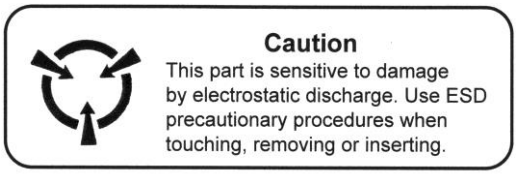
Register 0x3d (GAIN_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
GAIN_Z<7:0>								RW	0x00

GAIN_Z<9:0>: sensitivity trimming bits for z channel, together with GAIN_Z<9:8>in 0x37<4:3> (total 10 bits).

ORDERING INFORMATION

Ordering Number	Temperature Range	Package	Packaging
QMA7981-TR	-40℃~85℃	LGA-12	Tape and Reel: 5k pieces/reel



CAUTION: ESDS CAT. 1B

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China Patents 201510000399.8, 201510000425.7, 201310426346.3, 201310426677.7, 201310426729.0, 201210585811.3 and 201210553014.7 apply to the technology described.